Improvement in the determination by 1/f noise measurements of the interface state distribution in polysilicon TFTs in relation with the compensation law of Meyer Neldel

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Abstract

Low-frequency (1/f) noise is studied in N-channel furnace solid phase crystallized (FSPC) and in laser solid phase crystallized (LSPC) polysilicon TFTs biased from weak to strong inversion. Noise analysis is supported by the theory of charge carrier trapping/detrapping at the interface tunnelling into gate oxide traps.

The distribution of interface trap states (N_T) is deduced from the number of carriers trapped into the oxide. Noise measurements for devices biased from weak to moderate inversion allow the determination of the distribution of deep level trap states associated with dangling bonds type defects (N_{Tdb}); whereas measurements from moderate to strong inversion give the distribution of shallow level trap states (N_{Tts}) associated with strained bonds defects. The noise analysis clearly shows that the slope of both exponential distributions equals to the reverse of the Meyer Neldel energy E_{MN} (0.035 eV and 0.055eV for FSPC and LSPC TFT respectively).

For LSPC devices the resulting distribution of interface states ($N_T=N_{Tdb}+N_{Tts}$) is one decade lower and it is attributed to the effects of the laser annealing on the active layer crystal quality.

I. INTRODUCTION

Electrical properties in polysilicon thin film transistors (TFTs) are strongly controlled by trapping effect at defects both located within the bulk of the polysilicon active layer [1] and at the gate insulator/active layer interface. Two main causes of bulk defects are usually invoked: dangling bonds and strained bonds corresponding to deep and shallow level trap states into the band gap respectively. The energy distributions of the corresponding trap states (N_T) are representative of both the gate oxide and the active layer qualities, and thus are related to the electrical properties of the devices. Two types of distributions are considered: Gaussian distribution with a maximum around the midgap (N_{Tdb}) and exponential band tailing (N_{Tts}) corresponding to dangling bonds and strained bonds type defects respectively [2,3]. Methods based on capacitance, resistivity, and conductance activation energy measurements exist to determine these distributions [4,5].

More recently two approaches based on low frequency (1/f) noise measurements in polysilicon TFTs were proposed [6,7]. In this case, for N-channel polysilicon TFTs, 1/f noise is assumed to be due to carrier fluctuations usually modelled by carriers trapping/detrapping (T/D) from slow oxide traps located close to the interface. In the first study [6] a model taking into account additional fluctuations of the potential barriers height induced by the carriers trapping effect at the grain boundaries was suggested, and thus the average oxide and grain boundary trap densities were deduced. In the second study [7], based on the tunnelling theory of carriers into oxide traps, a method to determine the energy distribution of the interface states into the band gap was presented. In these two studies it was shown that 1/f noise level is strongly dependent on both interface and active layer qualities, and thus on fabrication process parameters. Therefore 1/f noise measurements can be used as a diagnostic tool to qualify TFT technology. However, the separated contributions of N_{Tdb} and N_{Tts} on the 1/f noise level in relation with the interface quality were not clearly demonstrated.

We present a study of 1/f noise level on polysilicon TFTs biased from weak to strong inversion. Analysis is based on carriers T/D from oxide traps and the separated contributions of deep and shallow level trap states on the resulting energy distribution of interface states in relation with the crystal quality of the active layer is presented. In addition, a direct relation with the Meyer Neldel effect [8] of N_{Tdb} and N_{Tts} is demonstrated, and it constitutes an improvement in the determination of the interface states distribution.

II. DEVICE AND EXPERIMENT DESCRIPTIONS

1/f noise is analysed on TFTs issued from two low-temperature ($\leq$ 600°C) technologies: Furnace Solid Phase Crystallized (FSPC) polysilicon TFTs and Laser Solid Phase Crystallized (LSPC) polysilicon TFTs.

Devices are fabricated on glass substrate. A thick APCVD (Atmospheric Pressure Chemical Vapour Deposition) SiO_2 layer is first deposited to prevent a possible contamination from the substrate because of severe thermal annealing during the fabrication process. FSPC TFTs (see fig. 1. a) are elaborated with one poly-Si layer: the upper part is heavily *in-situ* n-type doped (source and drain regions), and the bottom part is undoped and is dedicated to the active layer. LSPC TFTs (see fig. 1. b) are fabricated with two poly-Si layers: the active layer is built in the undoped layer, whereas an *in-situ* n-type doped layer constitutes source and drain regions. For the two types of TFTs the polysilicon layers are deposited by LPCVD (Low Pressure-CVD) technique and are crystallized by a FSPC thermal annealing in vacuum at 600°C. For LSPC structures an additional SPC thermal annealing of the active layer is carried out by using a scan of an Ar laser beam. Laser annealing parameters, power beam (P=4.8W) and scan speed (v=70mm/s), were adjusted to limit contamination of the active layer from the glass substrate. Under these conditions the active layer remains in solid phase and does not present a high degree of crystal quality as usually provided by other types of laser crystallization processes. Moreover, a possible contamination from the glass

substrate has been reported in such laser annealed polysilicon layer [9]. The gate insulator is made of a SiO_2 layer deposited by atmospheric pressure CVD (APCVD) technique at 390°C and annealed in nitrogen ambient for densification. The thickness of the gate oxide is 60nm and 50nm in SPC TFT and in LSPC TFT respectively. Electrodes are made of thermally evaporated aluminium. Finally, the devices were annealed into forming gas at 390°C.

Noise measurements are carried out in a shielded environment by using a low noise transimpedance amplifier (EG&G 5182, 15fA/$\sqrt{Hz}$) connected to the source electrode, followed by a low noise voltage amplifier (EG&G 5113, 4nV/$\sqrt{Hz}$) and a HP 3562A dynamic signal analyzer. A HP 4156 B semiconductor parameter analyzer is used for static drain current measurements. All tested devices are biased in the linear mode (V_{DS}=300mV) and operating from weak to strong inversion.

III-THEORETICAL ANALYSIS

It is widely admitted that in MOS transistors 1/f noise is due to channel conductivity fluctuation. Two mechanisms are proposed to explain it: i) carrier number fluctuation (ΔN model) or ii) carrier mobility fluctuation ($\Delta\mu$ model). ΔN model is based on carriers Generation-Recombination (G-R) processes at defects. In this case 1/f noise is explained as a superposition of G-R spectra with a distribution of time constant associated with carriers trapping/detrapping processes into the gate oxide. This noise model was first suggested by Mc Worther [10]. $\Delta\mu$ model describes mobility fluctuation due to scattering mechanisms of carriers in homogeneous samples of high crystal quality, and it is proposed by Hooge [11]. There have been ample discussions concerning the origin of the 1/f noise but they have not been decisive. Some effects can be explained by either models, but none of them can be definitively excluded.

A. Carriers trapping/detrapping process at oxide traps

It is widely admitted that low frequency noise in N-channel MOS transistors is due to carrier fluctuations. In this case, it can be described by the usual Hooge empirical relation of the normalized noise spectral density:

$$\frac{S_{I_{DS}}}{I_{DS}^2} = \frac{S_N}{N^2} = \frac{\alpha}{fN} \tag{1}$$

where S_{IDS} is the drain current power noise spectra density, S_N the carrier number power noise spectra density, I_{DS} the drain current, α the noise parameter and N the free carrier number. In addition, according to the G-R model the low frequency noise due to carrier fluctuations is described by [12]:

$$S_N(f) \propto \int_{\tau_0}^{\tau_1} \frac{d\tau}{1+(2\pi f\tau)^2} \propto \frac{[\arctan 2\pi f\tau]_{\tau_0}^{\tau_1}}{2\pi f} \tag{2}$$

with f the frequency and τ_0 (τ_1) the lower (upper) limit of time constants involved in the carriers T/D processes at defects. In this case 1/f noise spectrum is obtained for $1/\tau_1 << f << 1/\tau_0$ it means for long time constant τ_1 (see fig. 2. a). For carriers T/D at SiO_2/poly-Si interface followed by tunnelling into oxide traps (see fig. 2. b) the time constant τ is expressed as $\tau=\tau_0\exp(y/\lambda)\exp((E_C-E)/kT)$ with λ is the tunnel attenuation distance (≈0.1nm) and $\tau_0 \sim 10^{-10}$s [13]. In this case maximum time constant τ_1 can be very long. For example, considering that maximum value of E_C-E can be half polysilicon band gap (0.56eV), and with y=2nm (typical oxide depth for simulated low frequency noise at f=1Hz) [13], $\tau_1 \sim 10^6$s. For carriers T/D at defects in the bulk of the polysilicon active layer $\tau = \tau_0\exp((E_C-E)/kT$, and the maximum time constant is much shorter ($\tau_1 \sim 0.003$s). In this case, bulk trap contribution cannot explain the 1/f noise spectra of S_{IDS}/I^2_{DS} measured for 1Hz≤f≤300Hz (0.03s≤τ≤1s) on both FSPC and LSPC TFTs biased from weak to strong inversion (see fig. 2 in ref [14]). Therefore, our 1/f noise analysis is supported by the theory

of carriers T/D processes at the interface tunnelling into gate oxide traps located close to the interface (Mc Worther model) related to long time constants.

Previous theoretical study [15] on the relevance of the Mc Worther model showed that theoretical behaviour of noise parameter α versus the gate voltage does not correspond to whose usually measured for crystalline MOS transistors. However, in the case of polysilicon TFTs, a previous experimental study [16] showed that α measurements follow theoretical predictions, and thus our noise analysis is based on the corresponding theoretical calculations α reported in ref [15].

In this study, calculations of α are carried out by considering the effective number m* defined by $1/m^*=1/m+1/(M-m)$ with m the number of trapped carriers into the oxide and M the number of traps uniformly distributed into the gate oxide. The number m is both controlled by the number of traps at the interface n_t, the oxide depth y, and the inversion free carrier number N. So, m can be expressed as $m(E,y)=\exp(-y/\lambda)f_t(1-f_t)n_t(E)N$, with $f_t=1/(1+\exp((E-E_F)/kT))$ the Fermi factor, E_F the Fermi level energy and E the trap energy [12]. Considering $M(E)=m(E,y)\times\exp(y/\lambda)$ and $m^*(E,y)=m(E,y)(1-\exp(-y/\lambda))$, therefore the average value of m* is:

$$m^*(E)\approx f_t(1-f_t)n_t(E)N\left(\frac{1}{t_{ox}}\int_0^{t_{0x}}(exp(-y/\lambda)-exp(-2y/\lambda))dy\right)\approx n_t(E)Nf_t(1-f_t)\lambda/2t_{ox} \qquad (3)$$

with t_{ox} the thickness of the gate oxide (typically>>λ).

Furthermore it has been reported that [15]:

i) for m*<<N, it means from weak to moderate inversion (at low gate voltages), trap occupancy is small and α increases as E_F increases into the lower part of the band gap following the N/m^* ratio and:

$$\alpha\approx 4\frac{N\lambda}{m^* t_{ox}} \qquad (4)$$

ii) for m*>>N, it means from moderate strong inversion (at high gate voltages), trap occupancy is high and α decreases as E_F increases into the upper part of the band gap following the m^*/N ratio and:

$$\alpha \approx \frac{m^* \lambda}{N t_{ox}} \tag{5}$$

with m^*(≈M-m) acting as the trapping centre number.

A previous experimental study of 1/f noise on polysilicon TFTs reported the validity of these theoretical results [16]. Our analysis is supported by relations (4) and (5) for the determination from $n_t(E)$ of the interface states energy distribution as described in the next section.

B. Interface trap states distribution

For the calculation of the interface trap states distribution in the TFTs, we assumed that the free carrier number $N \approx N_C W L t_{si} \exp((E_F-E_C)/kT)$ with N_c ($\sim 10^{19} cm^{-3}$) the effective density of states into the conduction band, W(L) the width(length) of the channel and t_{si} (=150nm for FSPC TFT and =100nm for FSPC TFT) the thickness of the active layer. Moreover, considering that when $E \leq E_F$ trap occupancy is high, in dynamical equilibrium $E_C-E_F \approx E_A-(E_F-E)$ (see fig 2. b), thus $N f_t(1-f_t)=(N_C W L t_{si})\exp(-E_A/kT)(1+\exp((E-E_F)/kT))^{-2}$. Then the calculation of n_t is possible and the corresponding interface trap states distribution N_T ($cm^{-2}\ eV^{-1}$) can be deduced considering traps within an energy band kT around the Fermi level ($1+\exp((E-E_F)/kT) \sim 2$) by stating $N_T=n_t/(WLkT)$.

Therefore, because thermal activation energy associated with T/D process is $E_A=E_C-E$, then for high values of E_A (low gate voltages) according to (2), (3) and (4) we deduce:

$$N_{Tdb}(E) \approx \frac{32}{(WL)^2 f N_C t_{si} kT} \frac{I_{DS}^2}{S_{I\,DS}} \exp\left(\frac{E_A}{kT}\right) \tag{6}$$

In addition, for low values of E_A (high gate voltages) according to (2), (3) and (5), we obtain:

$$N_{Tts}(E) \approx \left(\frac{t_{ox}}{\lambda}\right)^2 \frac{8fN_C t_{si}}{kT} \frac{S_{I\,DS}}{I_{DS}^2} \exp\left(-\frac{E_A}{kT}\right) \tag{7}$$

These two relations allow the calculation of the interface trap states distribution from E_A and S_{IDS}/I^2_{DS} both deduced from measurements of I_{DS} and S_{IDS} at various gate voltages. Significant values of N_{Tdb} correspond to deep level trap states distribution (high values of E_A) assumed to be related to dangling bond type defects, whereas N_{Tts} significant values correspond to shallow level ones (low values of E_A) associated with strained bond defects (band tailing). Thus the resulting interface trap states distribution (N_T) is $N_T = N_{Tdb} + N_{Tts}$.

IV. EXPERIMENTAL ANALYSIS

A. Temperature dependence

Previous experimental studies [17,18] reported that the static drain current I_{DS} and the 1/f noise drain current spectral S_{IDS}, for TFTs biased from weak to strong inversion, (ie from sub- to above-threshold region) are thermally activated both following the empirical Meyer Neldel (MN) rule [8] according to:

$$\begin{cases} I_{DS} = I_{DS0} exp\left(\frac{E_A}{E_{MN}}\right) exp\left(-\frac{E_A}{kT}\right) \\ I_{DS0} = \beta_0(V_{DS})(V_{GS} - V_0) \end{cases} \tag{8}$$

and

$$S_{IDS} \approx S_{IDS0} \exp\left(\frac{E_A}{E_{MN}}\right) \exp\left(-\frac{E_A}{kT}\right) \tag{9}$$

with E_{MN} the MN characteristic energy, V_0 the gate voltage corresponding to the minimum of the drain current on the transfer characteristics plotted in a semi-logarithmic scale, and $\beta_0(V_{DS})$ the transconductance. Meyer Neldel effect is related to the multiple trapping processes of carriers [19], and in our case it is assumed to be the dominant carrier transport mechanism mainly occurring at the interface along the channel. It was also reported that the E_{MN} could act as a factor of merit of

the quality of the polysilicon active layer depending on the process fabrication parameters such as pressure deposition [17]. Moreover, it was shown that E_{NM} is related to exponential distribution of tail states [20], and that its slope becomes steeper as E_{MN} decreases [21]. In addition, study of numerical simulation of static drain current showed that MN effect is mainly controlled by the trap distribution associated with defects located at the gate insulator/active layer interface [22]. Values of E_{MN} parameters are mentioned in the table I for FSPC and LSPC TFTs, and the plots of the corresponding activation energies versus the gate voltage are reported in the figure 3.

B. Results

Plots of $I_{DS}=f(V_{GS})$ and $S_{IDS}/I^2_{DS}=f(I_{DS})$ of the studied devices (operating in the linear mode) are displayed in the figures 4 and 5 respectively. The corresponding interface trap states distributions are then calculated according to (6) and (7) and reported in a semi logarithmic scale in the figure 6. The resulting interface trap states distributions N_T exhibits a linear increase for shallow level traps (strained bonds type defects) and a linear decrease for the deep levels into the band gap (dangling bonds type defects). The expected maximum of the deep states distribution usually depicted around the midgap is not observed and should be extrapolated. Indeed, the maximum of N_T corresponds to the maximum value of E_A measured around the minimum value of I_{DS} (*ie* below 10^{-9}A) but noise measurements for devices biased at such low level of the drain current is difficult. Furthermore, for LSPC TFTs plot of N_T shows a deviation from exponential distribution versus activation energy at shallow trap levels (fig 6. (b)). This can be explained by the (source/drain) access resistances 1/f noise contribution at high gate voltage (low activation energy). Indeed, this contribution is particularly pronounced for LSPC device due to the existing active layer/source(drain) region interface, that does not appear in FSPC TFTs, and acting as additional source of noise [23]. Moreover, previous work [24] reported that at high gate voltages the access resistances noise contribution (S_{Rac}) dominates channel noise, whereas the resistance of the channel (R_c) is still

higher than the value of the total access resistance (R_{ac}). Under these conditions, in the linear mode, the total resistance (R) is $R=R_c+R_{ac,}\approx R_c$ and the resistance power spectra density (S_R) is $S_R=S_{Rc}+S_{Rac}\approx S_{Rac}$, with S_{Rac} non dependant on the gate voltage. Thus, the normalized noise becomes $S_{IDS}/I^2_{DS}=S_R/R^2\propto\exp(-2(E_A/kT-E_A/E_{MN}))$, whereas $S_{IDS}/I^2_{DS}\propto\exp(E_A/kT-E_A/E_{MN})$ without access resistances noise contribution. Therefore, determination of N_T considering the access resistance noise contribution gives, according to (7), an exponential distribution at shallow trap levels with a lower slope for LSPC TFTs (fig. 6 (b)). Because our model is based on the domination of the channel noise, it is not applicable for determination of shallow level interface trap states distribution in the case of access resistances noise contribution within TFTs at high gate voltages.

In order to avoid this discrepancy in determination of N_{Tts}, improved formulation can be given by injecting (8) and (9), into (6) and (7). Therefore, with $E_A=E_C-E$ (see fig. 2. b) (6) and (7) respectively become:

$$N_{Tdb}(E)\approx N_{Tdb0}\exp\left(\frac{E_C-E}{E_{MN}}\right) \tag{10}$$

with $N_{Tdb0}=32I^2_{DS0}/(fN_C(WL)^2t_{si}kTS_{IDS0})$ and

$$N_{Tts}(E)\approx N_{Tts0}\exp\left(-\frac{E_C-E}{E_{MN}}\right) \tag{11}$$

with $N_{Tts0}=8(t_{ox}/\lambda)^2fN_Ct_{si}S_{IDS0}/(I^2_{DS0}kT)$. In this case the determination of the resulting interface states distribution given by (10)+(11) can be deduced from measurements of the drain current activation energy at different gate bias, and from the saturated value of the normalized drain current noise spectra, S_{IDS0}/I^2_{DS0}, measured at high gate bias (*ie* for $E_A<<kT$) (see inset of the fig. 5). Furthermore, these two relations show the direct dependence of the interface trap states density on the MN characteristic energy, and valid the results of the numerical simulation of the static conduction in polysilicon TFTs reporting the strong dependence of the MN effect on the trap states

distribution related to defects located at the interface [22]. In addition, equations (10) and (11) agree with the two exponential distributions of trap state model used for the theoretical studies to correlate the Meyer Neldel effect with the statistical shift of the Fermi level within the density of states distribution [20,25].

In the figure 7 plots of the resulting interface states densities deduced from (10)+(11) are reported with those obtained according to (6)+(7) for the two types of TFTs. By applying (10) and (11) we can observe a good agreement with (6) and (7) except at shallow levels for LSPC TFTs (because of the access noise effect as previously mentioned). Differences in values of N_T between the two methods of calculations is less than one decade and can be explained by induced estimation errors such as geometry (W, L, t_{ox}) and E_{MN} parameters. In addition, because measurements from static drain current activation energy is possible at low current level corresponding to high activation energy values (see fig. 3 and 4), determination of N_T given by (10) and (11) allows a calculation over a larger range of trap levels, and more particularly close to the midgap. The results highlight that the density of the interface states is significantly lower for LSPC devices, and more particularly for deep states into the band gap corresponding to a lower density of dangling bonds type defects. This result is attributed to a better quality of the interface in relation with the improved crystal quality of the active layer due to the laser annealing.

In polysilicon films, the energy distribution of trap states can be modelled by the sum of a deep level Gaussian distribution $N_{ds}(E)$ with a maximum at energy E_t near the midgap, and an exponential-like $N_{ts}(E)$ band tail near the conduction band edge following [2,3]:

$$N_T(E) = N_{ds}(E) + N_{ts}(E) = \frac{N_d}{\sqrt{2\pi}s_d}\exp\left(-\frac{(E-E_t)^2}{2s_d^2}\right) + N_s\exp\left(-\frac{E_c-E}{kT_s}\right) \qquad (12)$$

where N_d is the total trap density per unit area, s_d the standard deviation of the Gaussian distribution, N_s and T_s the characteristic parameters of the exponential trap distribution. These distributions can be related to distributions given by (10) and (11). Indeed, for shallow level

interface trap states distribution, parameters are clearly linked by standing $N_S=N_{Tts0}$ and $kT_s=E_{MN}$. For deep level interface trap states distribution the link is less evident, but considering the maximum of the distribution (N_{Tdbmax}) close to the midgap, it means with $E_A=E_C-E\approx E_G/2$ ($\approx$0.56eV), thus $N_{Tdbmax}=N_{Tdb0}\exp(E_G/(2E_{MN}))=N_d/(\sqrt{2\pi s_d})$. As S_{IDS0}/I^2_{DS0} and E_{MN} parameter values depend on process fabrication parameters [17], it shows the link of the interface deep state distribution parameters with the gate insulator interface and the active layer qualities. For our studied devices, N_{Tts0} and N_{Tdbmax} were estimated according to (10) and (11) and are summarized in the table I. The values are convenient with previous published results [2, 3].

These results show the dependence of the shape of the interface trap states distribution on the E_{MN} parameter in relation with the quality of the interface. Our study validates the steeper slope of the exponential tail state distribution as E_{MN} decreases as previously reported [2,21]. In addition, it confirms i) the change of E_{MN} value in function of the polysilicon active layer quality [17], and ii) the strong influence of the interface trap states distribution on the Meyer Neldel effect for the drain current thermal activation [22].

IV. CONCLUSION

In this experimental analysis of the 1/f noise we emphasized the influence of the interface quality in polysilicon TFTs on specific description of noise. A new method is proposed to determine the energy distribution of the interface trap states in polysilicon TFTs from the 1/f noise measurements. It is based on the variations of the normalized drain current spectral density with the gate voltage. Two regimes of variations are considered corresponding respectively to the weak and the strong inversion regions.

1/f noise spectrum at low frequency is explained by the domination of the carriers trapping/detrapping process from defects located at the interface tunnelling into oxide traps. The contributions of related band tailing (strained bonds) and dangling bonds interface defects are

separately estimated. Quantitative dependence, in relation with the interface quality, and thus with the TFT-technology, on the Meyer Neldel energy parameter of the two corresponding exponential distributions is shown. For LSPC TFT, both tails and dangling bonds states distributions are wider because of a higher Meyer Neldel energy, and the resulting interface trap states density is one decade lower than for FSPC TFT due to the effect of the laser annealing on the crystal quality of the active layer.

The study confirms the validity of the tunnelling theory of trapped carriers into the gate oxide (Mc Worther theory) to explain 1/f noise in polysilicon TFTs.

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Table caption

Table I: summary of interface state distribution parameters for the FSPC and the LSPC TFTs.

	E_{MN} (eV)	N_{Tts0} (cm^{-2} eV^{-1})	N_{Tdbmax} (cm^{-2} eV^{-1})
FSPC TFT	0.035	$\sim 10^{15}$	$\sim 8\times 10^{13}$
LSPC TFT	0.055	$\sim 10^{13}$	$\sim 3\times 10^{11}$

Figure captions

Figure 1: Cross section of the tested devices: (a) FSPC TFT, (b) LSPC TFT

Figure 2: (a) Schematic theoretical low frequency noise spectrum for G-R model: 1/f noise spectrum (dotted line) can be obtained for long time constant τ_1 associated with T/D processes of carriers into slow oxide traps. (b) Band bending at the interface in N-channel MOS transistor under a positive gate voltage; dotted lines illustrate trapping/detrapping process of carrier tunnelling into the oxide trap energy E. A shallow traps levels close to the conducting band, B deep trap levels around the midgap.

Figure 3: Plots of E_A versus V_{GS} the FSPC and LSPC TFTs.

Figure 4: Transfer characteristics plotted in the linear mode (V_{DS}=300mV) of the tested FSPC TFTs (W/L=30µm/10µm) and the LSPC TFTs (W/L=80µm/60µm).

Figure 5: Normalized drain current noise spectral density versus drain current for: (a) FSPC TFTs, (b) LSPC TFTs, (f=10 Hz, V_{DS}=300mV). Inset: same plots in semi logarithmic scale.

Figure 6: Plots of the interface trap state densities deduced from (5) and (6) for: (a) FSPC TFTs, (b) LSPC TFTs.

Figure 7: Plots of the interface trap state distributions deduced from noise measurements given by (5)+(6) and by (9)+(10) for FSPC and LSPC TFTs. Dotted plots: extrapolated interface trap state distributions deduced from static drain current activation energy given (9)+(10).